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Claims

[c1] What is claimed is:

1.A via-first dual damascene process, comprising:

providing a semiconductor substrate having a conductive structure and a dielectric layer on the semiconductor substrate, wherein the dielectric layer has a via opening exposing the conductive structure;

filling the via opening with a gap-filling polymer to form a gap-filling polymer (GFP) layer on the dielectric layer;

etching the GFP layer back to a predetermined depth such that an exposed surface of the GFP layer is lower than surface of the dielectric layer to form a recess, thereby exposing portions of sidewalls of the via opening; and

performing a surface treatment for altering surface property of the sidewalls and the exposed surface of the GFP layer, thereby preventing a subsequent deep UV photoresist from interacting with the sidewalls or the exposed surface of the GFP layer either in a chemical or physical way.

[c2] 2.The via-first dual damascene process of claim 1 wherein the GFP layer is composed of an i-line resist.

[c3] 3.The via-first dual damascene process of claim 1 wherein the dielectric layer has a dielectric constant of less than 3.0.

[c4] 4.The via-first dual damascene process of claim 1 wherein an etching stop layer is provided on the dielectric layer.

[c5] 5.The via-first dual damascene process of claim 4 wherein the etching stop layer is made of silicon oxynitride.

[c6] 6.The via-first dual damascene process of claim 1 wherein the surface treatment means is using active radicals having a relatively low etching rate (with respect to the GFP layer) to contact the sidewalls and the exposed surface of the GFP layer.

[c7] 7.The via-first dual damascene process of claim 6 wherein the relatively low etching rate is less than 100 Å/min.

[c8] 8.The via-first dual damascene process of claim 6 wherein the active radicals comprises oxygen radical and superoxide radical.

[c9] 9.The via-first dual damascene process of claim 6 wherein the by using active radicals having a relatively

low etching rate (with respect to the GFP layer) to contact the sidewalls and the exposed surface of the GFP layer, the exposed surface of the GFP layer is transformed into a hydrophilic surface.

[c10] 10.The via-first dual damascene process of claim 1 wherein the surface treatment means is depositing a conformal polymer film over the sidewalls and the exposed surface of the GFP layer.

[c11] 11.The via-first dual damascene process of claim 10 wherein the polymer film is deposited by using a plasma composition of CHF_3/H_2 or CF_4/CHF_3.

[c12] 12.The via-first dual damascene process of claim 10 wherein the thickness of the polymer film is about 50 angstroms to 150 angstroms.

[c13] 13.A via-first dual damascene process, comprising:
providing a semiconductor substrate having a conductive structure and a dielectric layer on the semiconductor substrate, wherein the dielectric layer has a via opening exposing the conductive structure;
filling the via opening with a gap-filling polymer to form a gap-filling polymer (GFP) layer on the dielectric layer;
etching the GFP layer back to a predetermined depth such that an exposed surface of the GFP layer is lower

than surface of the dielectric layer to form a recess, thereby exposing portions of sidewalls of the via opening;

performing a surface treatment for unifying surface condition of the sidewalls and the exposed surface of the GFP layer;

filling the recess with a deep UV (DUV) photoresist to form a DUV photoresist layer on the dielectric layer;

performing a lithographic process to form a trench opening in the DUV photoresist layer above the via opening; and

etching the dielectric layer and the GFP layer through the trench opening using the DUV photoresist layer as an etching mask.

[c14] 14.The via-first dual damascene process of claim 13 wherein the GFP layer is composed of an i-line resist.

[c15] 15.The via-first dual damascene process of claim 13 wherein the dielectric layer has a dielectric constant of less than 3.0.

[c16] 16.The via-first dual damascene process of claim 13 wherein an etching stop layer is provided on the dielectric layer.

[c17] 17.The via-first dual damascene process of claim 13

wherein the surface treatment means is using active radicals having a relatively low etching rate (with respect to the GFP layer) to contact the sidewalls and the exposed surface of the GFP layer.

[c18] 18.The via-first dual damascene process of claim 17 wherein the relatively low etching rate is less than 100 Å/min.

[c19] 19.The via-first dual damascene process of claim 17 wherein the active radicals comprises oxygen radical and superoxide radical.

[c20] 20.The via-first dual damascene process of claim 17 wherein by using active radicals having a relatively low etching rate (with respect to the GFP layer) to contact the sidewalls and the exposed surface of the GFP layer, the exposed surface of the GFP layer is transformed into a hydrophilic surface.

[c21] 21.The via-first dual damascene process of claim 13 wherein the surface treatment means is depositing a conformal polymer film over the sidewalls and the exposed surface of the GFP layer.

[c22] 22.The via-first dual damascene process of claim 21 wherein the polymer film is deposited by using a plasma composition of CHF_3/H_2 or CF_4/CHF_3.

[c23] 23.The via-first dual damascene process of claim 21 wherein the thickness of the polymer film is about 50 angstroms to 150 angstroms.